Features

- **Reference Oscillator up to 15 MHz**
- **Two Programmable 16-bit Dividers Adjustable from 2 to 65535**
- **Fine Tuning Steps**
  - **AM ≥ 1 kHz**
  - **FM ≥ 2 kHz**
- **Loop-push-pull Stage for AM/FM**
- **High Signal/Noise Ratio**

Pb Lead Free

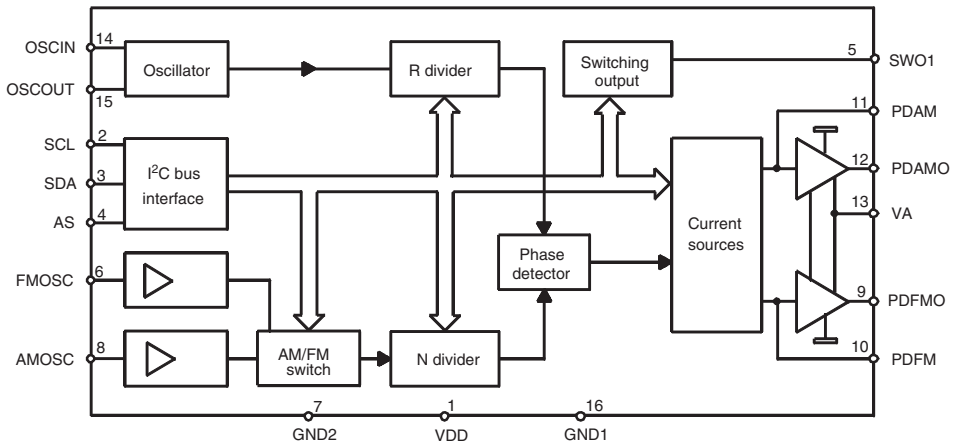
AM/FM PLL with 1 Switch

ATR4289

1. Description

The ATR4289 is an integrated circuit in BiCMOS technology for frequency synthesizers. It performs all the functions of a PLL radio tuning system and is controlled by a 2-wire bus. The device is designed for all frequency synthesizer applications in radio receivers, as well as for radio data system (RDS) applications.

Figure 1-1. Block Diagram



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2. Pin Configuration

Figure 2-1. Pinning SO16

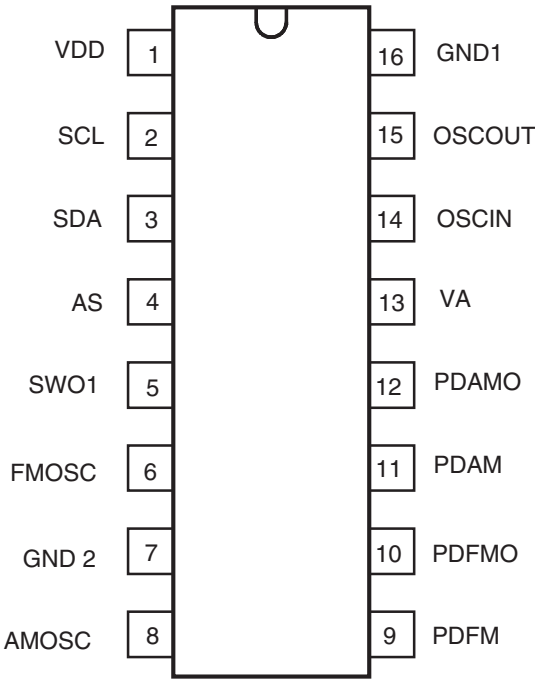


Table 2-1. Pin Description

Pin	Symbol	Function
1	VDD	Supply voltage
2	SCL	Bus clock
3	SDA	Bus data
4	AS	Address selection
5	SWO1	Switching output
6	FMOSC	FM oscillator input
7	GND2	Ground 2 (analog)
8	AMOSC	AM oscillator input
9	PDFM	FM current output
10	PDFMO	FM analog output
11	PDAM	AM current output
12	PDAMO	AM analog output
13	VA	Analog supply voltage
14	OSCIN	Oscillator input
15	OSCOUT	Oscillator output
16	GND1	Ground 1 (digital)

3. Functional Description

The ATR4289 is controlled via the 2-wire bus. One module-address byte, two subaddress bytes and five data bytes enable programming.

The module address contains a programmable address bit A 1, which (along with address select input AS, pin 4), enables the operation of two ATR4289 devices in one system. If bit A 1 is identical with the status of the address select input AS, the chip is selected.

The subaddress determines which of the data bytes is transmitted first. If the subaddress of the R divider is transmitted, the sequence of the next data bytes is DB 0 (Status), DB 1 and DB 2. If the subaddress of the N divider is transmitted, the sequence of the next data bytes is DB 3 and DB 4. The bit organization of the module address, subaddress and 5 data bytes is shown in Table 7-1 on page 8.

Each transmission on the bus begins with the *START* condition and has to be ended by the *STOP* condition (see Table 8-1 on page 8, "Transmission Protocol").

The integrated circuit ATR4289 has two separate inputs for the AM and FM oscillators. Preamplified AM and FM signals are fed to the 16-bit R divider via the AM/FM switch. The AM/FM switch is software controlled. Tuning steps can be selected by the 16-bit R divider.

Furthermore, the device provides a digital memory phase detector and two separate current sources for the AM and FM amplifier (charge pump) as given in the Table "Electrical Characteristics" on page 5. It allows independent gain adjustment, providing high current for high-speed tuning and low current for stable tuning.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pins	Symbol	Value	Unit
Supply voltage	1	V_{DD}	–0.3 to +6	V
Input voltage	2, 3, 4, 6, 8, 14, 15	V_I	–0.3 to V_{DD} + 0.3	V
Output current	3, 5	I_O	–1 to +5	mA
Output drain voltage	5	V_{OD}	15	V
Analog supply voltage with 220Ω serial resistance 2 minutes[1]	13	V_A V_A	6 to 15 24	V V
Output current	9, 12	I_{AO}	–1 to +20	mA
Ambient temperature range		T_{amb}	–30 to +85	°C
Storage temperature range		T_{stg}	–40 to +125	°C
Junction temperature		T_j	125	°C
Electrostatic handling (modified MIL STD 883 D method 3015.7: all supply pins connected together)		$\pm V_{ESD}$	1000	V

Note: 1. Corresponding to the application circuit (Figure 9-1 on page 9)

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	160	K/W

6. Electrical Characteristics

V_{DD} = 5V, V_A = 10V, T_{amb} = 25°C, unless otherwise specified

Parameters	Test Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		1	V_{DD}	4.5	5.0	5.5	V
Quiescent supply current	AM mode/FM mode	1	I_{DD}		4.0	7.0	mA
FM input sensitivity, R_G = 50Ω, FMOSC	f_i = 70 MHz to 120 MHz	6	V_{SFM}	40			mV_{rms}
	f_i = 160 MHz	6	V_{SFM}	150			mV_{rms}
AM input sensitivity, R_G = 50Ω, AMOSC	f_i = 0.6 MHz to 35 MHz	8	V_{SAM}	40			mV_{rms}
Oscillator input sensitivity, R_G = 50Ω, OSCIN	f_i = 0.1 MHz to 15 MHz	14	V_{SOSC}	100			mV_{rms}
Phase Detector PDFM							
Output current 1		10	$\pm I_{PDFM}$	1600	2000	2400	µA
Output current 2		10	$\pm I_{PDFM}$	400	500	600	µA
Leakage current		10	$\pm I_{PDFML}$			20	nA
Phase Detector PDAM							
Output current 1		11	$\pm I_{PDAM}$	160	200	240	µA
Output current 2		11	$\pm I_{PDAM}$	40	50	60	µA
Leakage current		11	$\pm I_{PDAML}$			20	µA
Analog Output PDFMO, PDAMO							
Saturation voltage LOW	I = 15 mA	9, 12	V_{satL}		200	400	mW
Saturation voltage HIGH	I = 15 mA	9, 12	V_{satH}	9.5	9.95		V
Bus SCL, SDA, AS							
Input voltage HIGH		2, 3, 4	V_{iBUS}	3.0		V_{DD}	V
Input voltage LOW		2, 3, 4	V_{iBUS}	0		1.5	V
Output voltage acknowledge LOW	I_{SDA} = 3 mA	3	V_O			0.4	V
Clock frequency		2	f_{SCL}			100	kHz
Rise time SDA, SCL		2, 3	t_r			1	µs
Fall time SDA, SCL		2, 3	t_f			300	ns
Period of SCL HIGH		2	t_H	4.0			µs
Period of SCL LOW		2	t_L	4.7			µs
Set-up Time							
Start condition			t_{sSTA}	4.7			µs
Data			t_{sDAT}	250			µs
Stop condition			t_{sSTOP}	4.7			µs
Time space[1]			t_{wSTA}	4.7			µs
Hold Time							
Start condition			t_{hSTA}	4.0			µs
Data			t_{hDAT}	0			µs

Note: 1. This is a period of time where the bus must be free from data transmission before a new transmission can be started.

Figure 6-1. FM Input Sensitivity, T_{amb} = +85°C

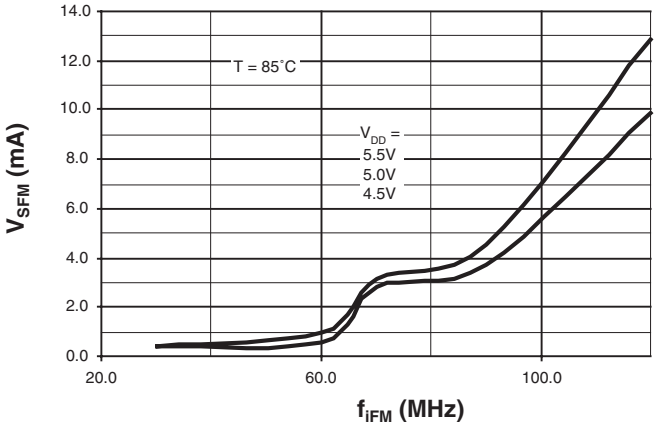


Figure 6-2. FM Input Sensitivity, T_{amb} = –30°C

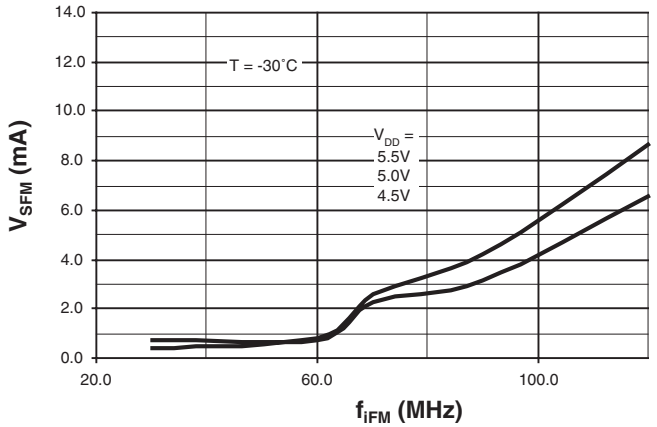


Figure 6-3. AM Input Sensitivity, T_{amb} = +85°C

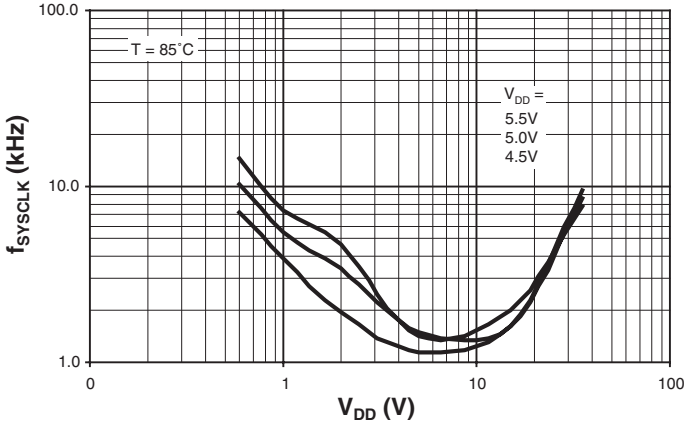


Figure 6-4. AM Input Sensitivity, T_{amb} = –30°C

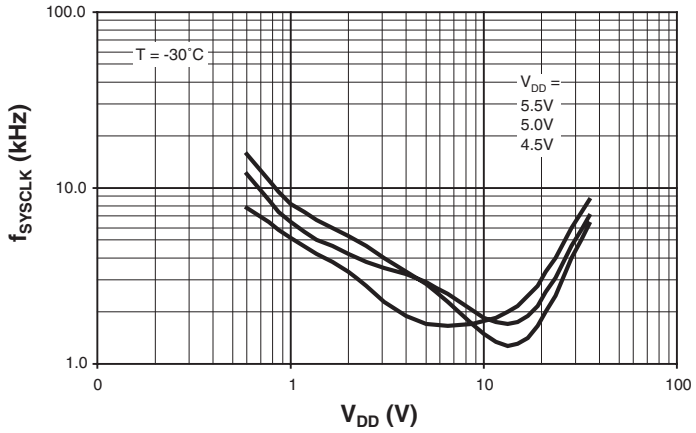
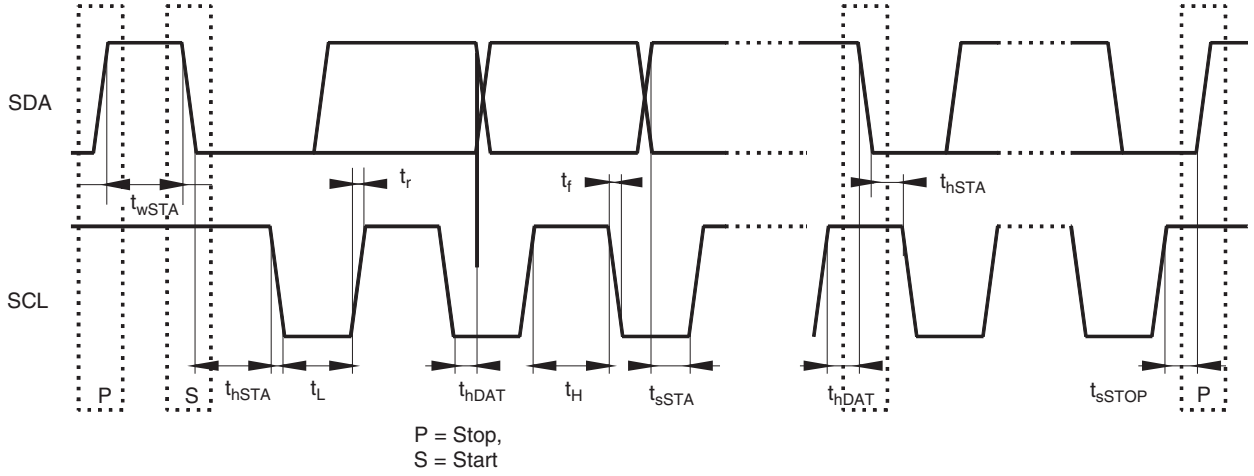


Figure 6-5. Bus Timing



7. Bit Organization

Table 7-1. Bit Organization

	MSB							LSB
Module address	1	1	0	0	1	0	0/1	0
	A7	A6	A5	A4	A3	A2	A1	A0
Subaddress (R-divider)	X	X	X	0	0	1	X	X
Subaddress (N-divider)	X	X	X	X	1	1	X	X
Data byte 0 (Status)	SWO1				AM/FM	PD - ANA	PD - POL	PD - CUR
	D7	D6	D5	D4	D3	D2	D1	D0
Data byte 1	2^{15}	R divider						2^{8}
Data byte 2	2^{7}	R divider						2^{0}
Data byte 3	2^{15}	N divider						2^{8}
Data byte 4	2^{7}	N divider						2^{0}

Table 7-2. Function Mode

Bit Description	Mode	LOW	HIGH
D3	AM/FM	FM operation	AM operation
D2	PD - ANA	PD analog	TEST
D1	PD - POL	Negative polarity	Positive polarity
D0	PD - CUR	Output current 2	Output current 1

8. Transmission Protocol

Table 8-1. Transmission Protocol

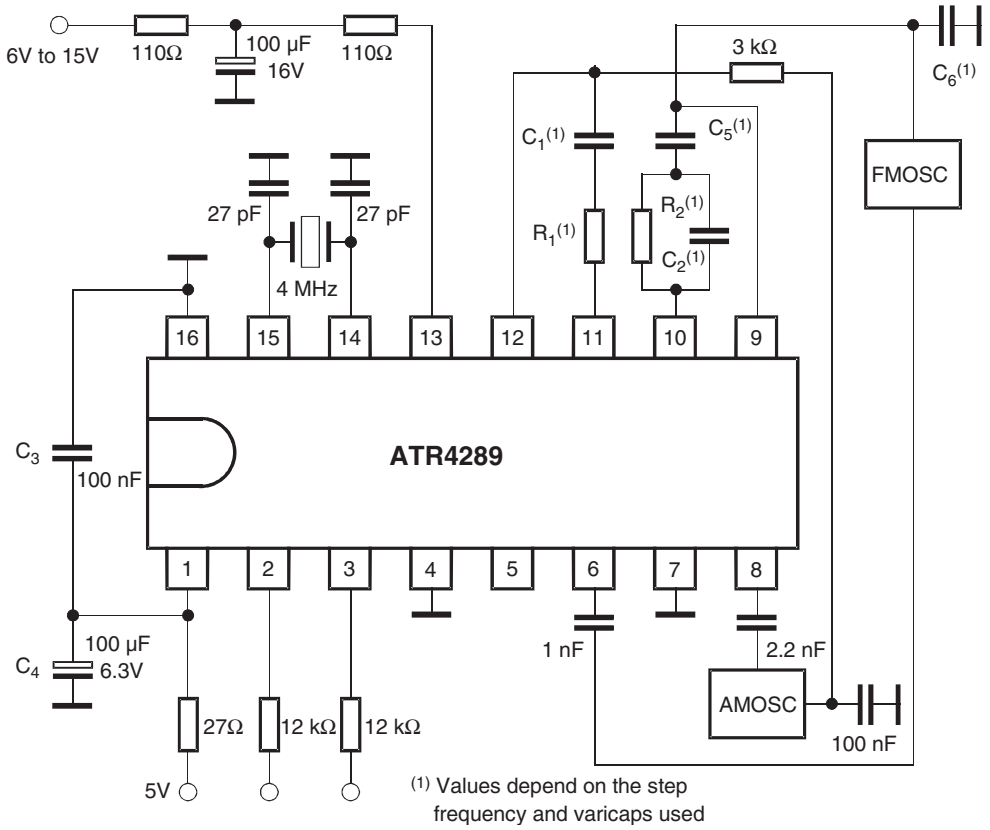
	MSB	LSB										
S	Address		A	Subaddress	A	Data 0	A	Data 1	A	Data 2	A	P
	A0	A7		R divider								

	MSB	LSB								
S	Address		A	Subaddress	A	Data 3	A	Data 4	A	P
	A0	A7		N divider						

Note: S = Start, P = Stop, A = Acknowledge

9. Application

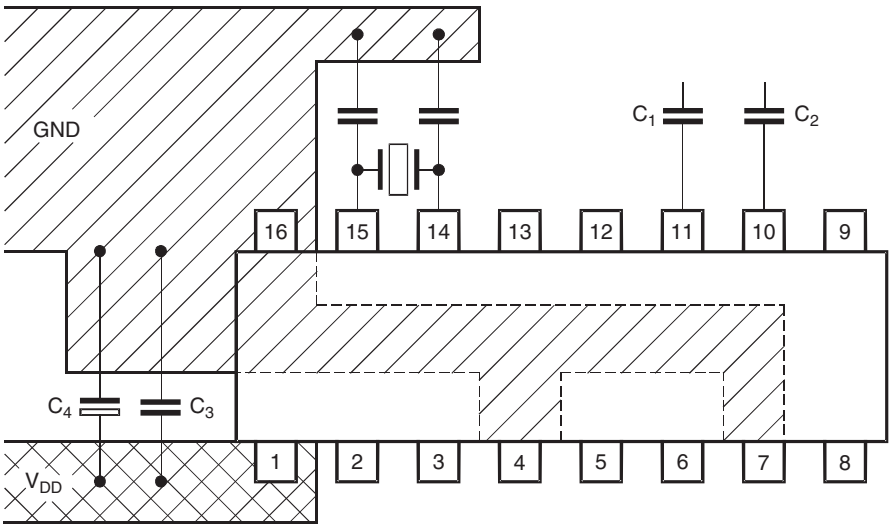
Figure 9-1. Application Circuit



9.1 Recommendations for Applications

- C_3 = 100 nF should be very close to pin 1 (V_{DD}) and pin 16 (GND1)
- GND2 (pin 7, analog ground) and GND1 (pin 16, digital ground) must be connected as shown in Figure 9-1
- 4 MHz crystal must be very close to pin 14 and pin 15
- Components of the charge pump (C_1 / R_1 for AM and C_2 / R_2 for FM) should be very close to pin 11 with respect to pin 10.

Figure 9-2. PCB Layout

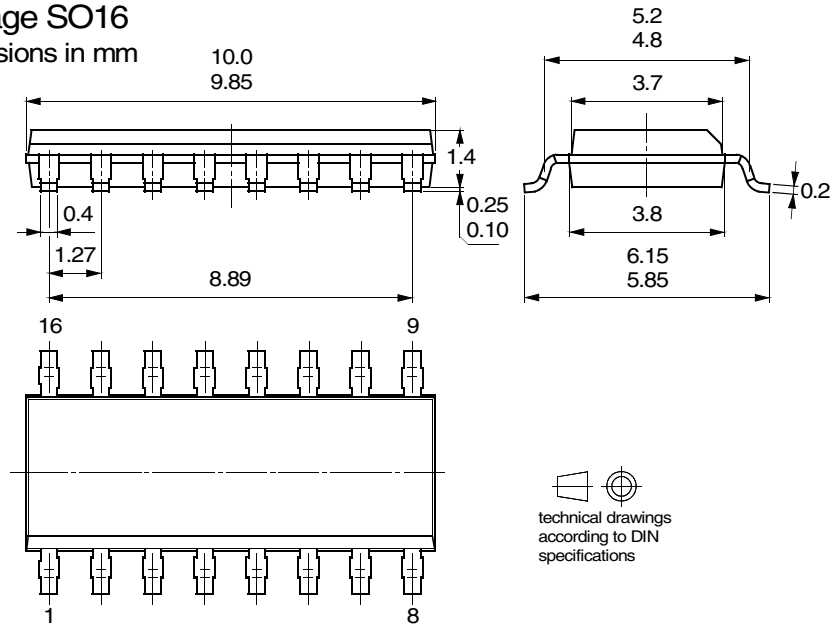


10. Ordering Information

Extended Type Number	Package	Remarks
ATR4289-TBSY	SO16 plastic	Pb-free
ATR4289-TBQY	SO16 plastic	Taping according to IEC-286-3, Pb-free

11. Package Information

Package SO16
Dimensions in mm



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